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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,562	04/01/2004	Chih-Hsin Ko	24061.176 (TSMC2003-1247)	1238

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,562	KO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,9-14,17-21,23,25-29,31,32 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 5-6, 9-14, 17-21, 23, 25-29, 31-32, 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 19-21 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for planarizing a dielectric film (130) [see figs. 1B-1D], does not reasonably provide enablement for forming a shallow trench isolation from such a planarization [see figs. 2B-2D]. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. It is noted that the embodiment disclosing the formation of the shallow trench isolation does not require such planarization step (figs. 2A-2D). Please note that this planarization step is used only for forming spacer (130) (see figs. 1A-1D).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 5-6, 9-14, 17-21, 23, 25-29, 31-32, 35-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Guarini et al. (US Pat. No. 6,830,962 B1).

Regarding claims 1, 13, 25-27, Guarini et al. teaches a microelectronic device, comprising:

a discrete first wafer bonded to a discrete second wafer (bonded SOI substrate) [see col. 3, lines 45-56 and col. 5, lines 10-25 and 63-68], wherein:

the first wafer comprises a first semiconductor substrate (16) [fig. 9], the second wafer comprises a second semiconductor substrate (12) [fig. 9], and the discrete first and second wafers are bonded such that the first semiconductor substrate and the second semiconductor substrate are proximate the bond between the discrete first and second wafers [consider the bonded structure shown in fig. 9];

one of the first and second semiconductor substrates has a (1,1,0) crystallographic orientation and the other of the first and second semiconductor substrates has a (1,0,0) crystallographic orientation [col. 4, lines 9-12 and 45-48]; and

an epitaxially grown portion of the second semiconductor substrate (28) extends through an opening (22) in the first wafer, including through the first semiconductor substrate (16) [see fig. 4 and col. 7, lines 10-14];

a shallow trench isolation (40) interposing a sidewall of the opening (22) and the epitaxially grown portion of the second semiconductor substrate (28), wherein the shallow trench isolation spans the thickness of the first wafer, including the first semiconductor substrate (16), and extends into the second semiconductor substrate (12) [see fig. 9 and col. 10, lines 9-10];

a first semiconductor device (50) coupled to the first semiconductor substrate (16) [see fig. 9]; and

a second semiconductor device (52) coupled to the epitaxially grown portion of the second semiconductor substrate (28) [see fig. 9].

Regarding claims 2, 14 and 28-29, Guarini et al. further teaches that one of the first and second semiconductor devices comprises a p-type transistor and the other of the first and second semiconductor devices comprises an n-type transistor [col. 10, lines 39-43].

Regarding claims 5, 17 and 31, Guarini et al. further teaches that the first semiconductor substrate has the (1,1,0) crystallographic orientation and the second semiconductor substrate has the (1,0,0) crystallographic orientation [col. 4, lines 9-12 and 45-48].

Regarding claims 6, 18 and 32, Guarini et al. further teaches that the first semiconductor substrate has the (1,0,0) crystallographic orientation and the second semiconductor substrate has the (1,1,0) crystallographic orientation [col. 4, lines 9-12 and 45-48].

Regarding claims 9-10, 23 and 35-36, Guarini et al. further teaches a silicon oxide layer (14) interposing the first semiconductor substrate (16) and the second wafer (12) [see fig. 9], the opening (22) also extending through the silicon oxide layer (14) [see fig. 2].

Regarding claims 11 and 37, Guarini et al. further teaches an implanted (SIMOX) oxide layer (14) interposing the first semiconductor substrate (16) and the second wafer

(12) [see fig. 9; and col. 2, lines 27-28], the opening (22) also extending through the implanted oxide layer (14) [see fig. 2].

Regarding claims 12 and 38, Guarini et al. further teaches that the first semiconductor substrate is a silicon-on-insulator substrate [col. 3, lines 45-46 and col. 5, lines 13-14].

Regarding claim 19, Guarini et al. further teaches forming a dielectric film (18) on the first wafer (16) opposite the second semiconductor substrate (12) before epitaxially growing the extension of the second semiconductor substrate (28) [see fig. 1].

Regarding claim 20, Guarini et al. further teaches planarizing the first wafer (16), the dielectric film (18), and the extension of the second semiconductor substrate (28) to form a substantially planar surface collectively therefrom [see figs. 4 and 8].

Regarding claim 21, Guarini et al. further teaches that planarizing includes substantially removing all of the dielectric film (18) not located in the opening (22) [see fig. 8].

Response to Arguments

4. Applicant's arguments with respect to claims 1-2, 5-6, 9-14, 17-21, 23, 25-29, 31-32, 35-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

José R. Díaz
Examiner
Art Unit 2815